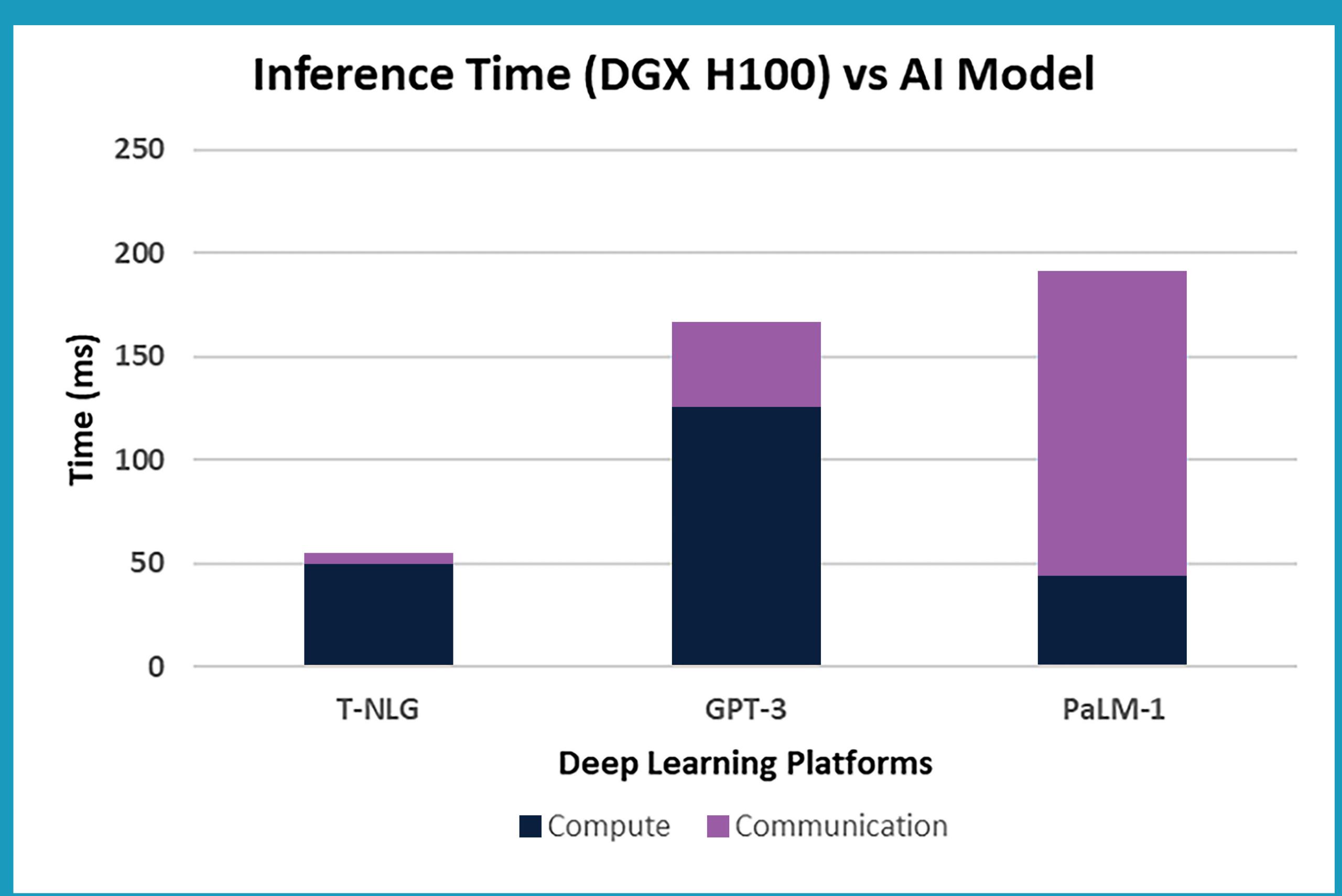# Driving Compute Scale-out Performance with Optical I/O Chiplets in Advanced System-in-Package Platforms

Mark Wade, Chen Sun, Matt Sysak, Vladimir Stojanović
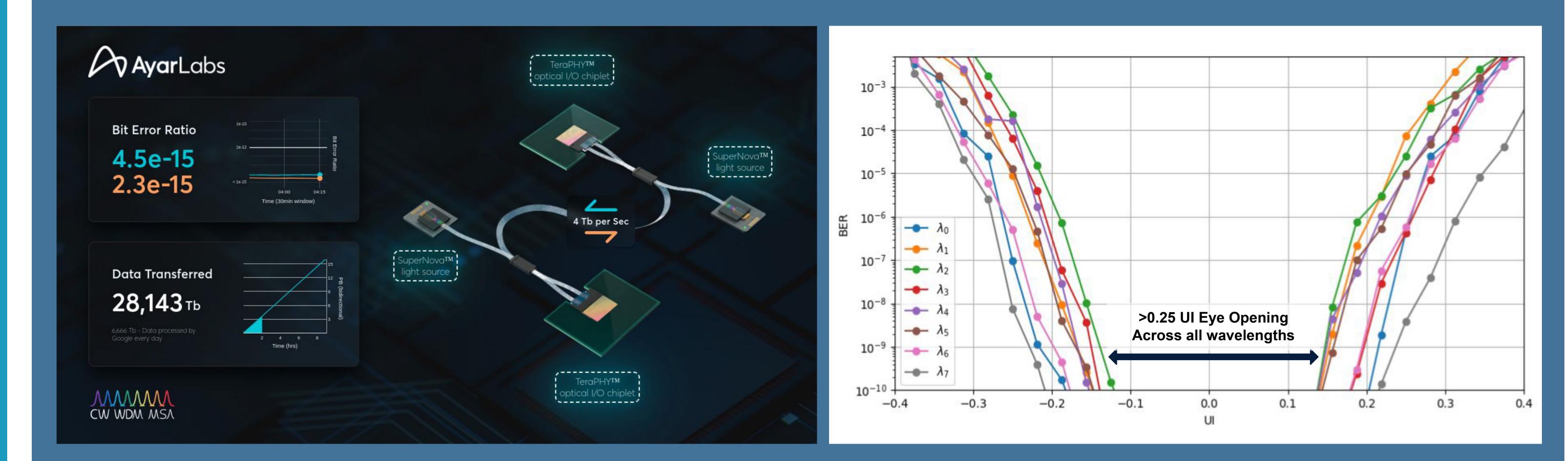Ayar Labs, Inc.
Santa Clara, CA, USA

Pooya Tadayon, Ravi Mahajan, Babak Sabi
Intel Foundry Services, Intel Corporation
Santa Clara, CA, USA
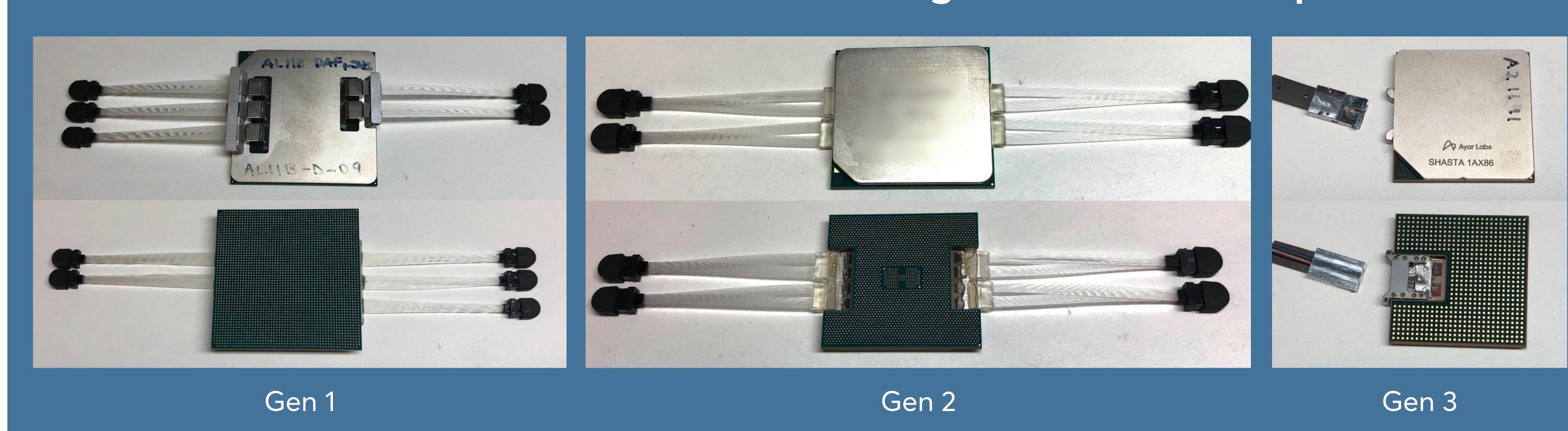
The Problem: The Package Escape Bandwidth Bottleneck

Inference Time (DGX H100) vs AI Model

Large scale models (>0.5T parameters) become dominated by communications across compute nodes.

Breaking the Bandwidth Bottleneck with Optical I/O

Socket – Socket
Board – Board
Rack - Rack

data

TeraPHY™ CMOS Optical I/O chiplet

SoC

Typical in-package temperature 80-110°C

2.5D or 2D package

Electrical I/O (parallel or serial)

SuperNova™ multi-port, multi-wavelength light source

laser

External laser module temperature <55°C
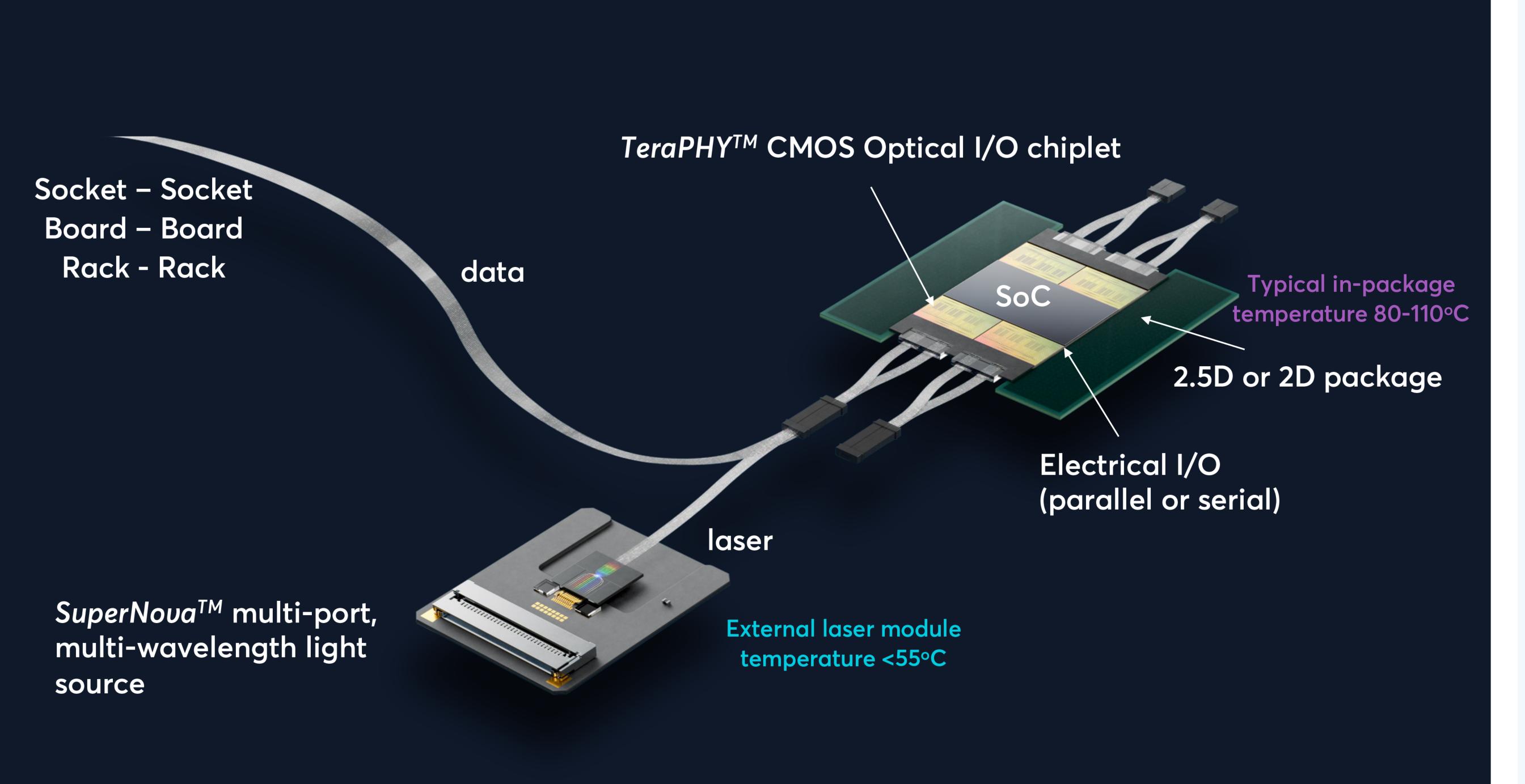
Results: 4 Tbps Optical I/O Chiplets Utilizing Advanced Packaging

>0.25 UI Eye Opening Across all wavelengths
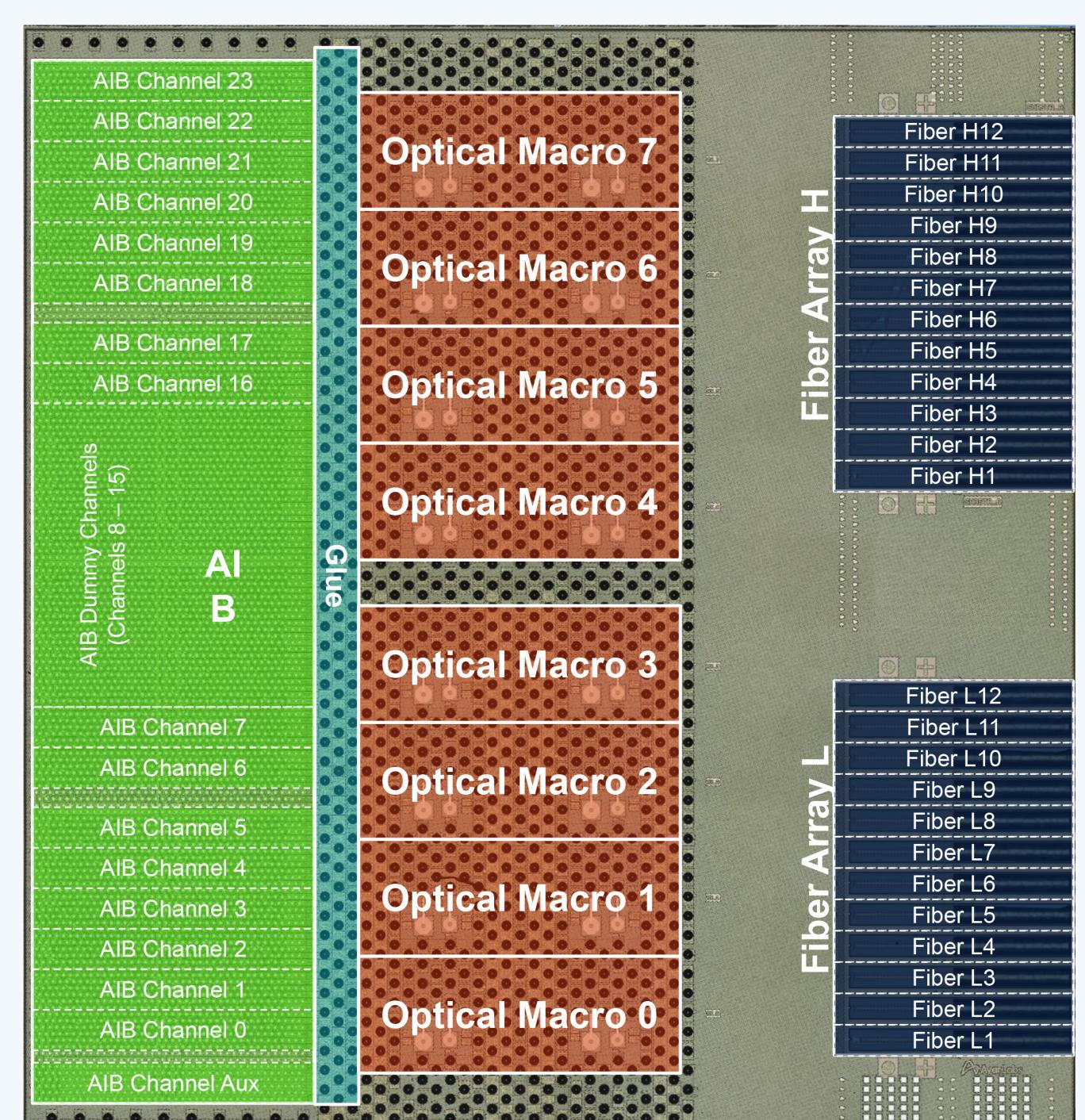
Evolution of Fiber Attach: Direct to Package Detachable Optical Fibers

Gen 1 | Gen 2 | Gen 3

A Roadmap to >250 Tbps Off-Package
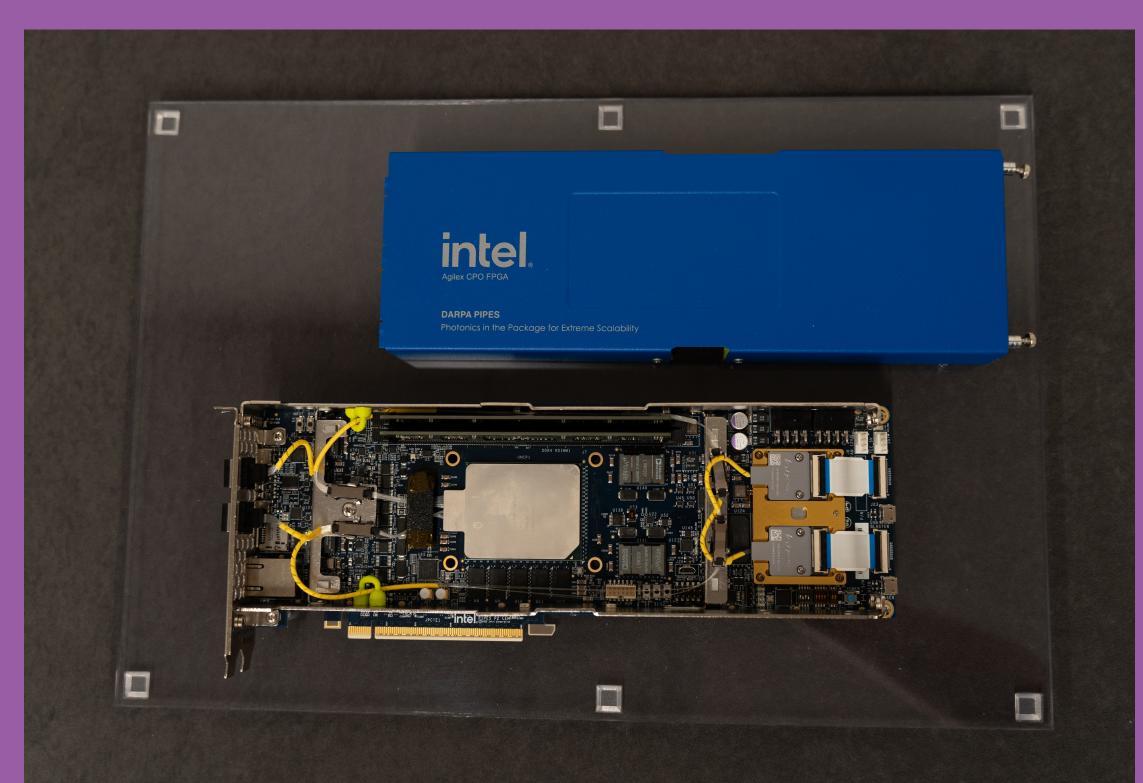
Gen	Electrical I/F (Advanced Package)				Optical I/F (CW-WDM)			Optical Chiplet BW (Tx+Rx)	Off-package IO BW (4-8 chiplets per package)
	I/F	Modules	Tx / Rx IOs	Data Rate [Gbps/IO]	Ports	λs / Port	Data Rate [Gbps/λ]		
1 [2]	AIB	24	20 / 20	2	8	8	16	2 Tbps	8-16 Tbps
2*	AIB	16	80 / 80	2	8	8	32	4 Tbps	16-32 Tbps
3	UCIe	16	32 / 32	8	8	16	32	8 Tbps	32-65 Tbps
4	UCIe	16	64 / 64	8	16	16	32	16 Tbps	65-131 Tbps
5	UCIe	16	64 / 64	16	16	16	64	32 Tbps	131-262 Tbps

Table 1: Generation roadmap for optical I/O chiplets. * indicates this work (Fig. 1, 2, 4)

Come See the Demo!

Ayar Labs' optical I/O solution integrated and working in the same package with Intel's Agilex FPGA PCIe card.